REMARKS

Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Allowable Claims

Applicants appreciate the indication that claims 19-23 and 44-46 contain allowable subject matter and would be allowed if presented in independent form. However, at this time, these dependent claims are not being presented in independent form because it is believed that the independent claims, from which they depend, are allowable. Moreover, Applicants submit that all claims are in condition for allowance for the following reasons.

35 U.S.C. §101 Rejection

Claims 1-33, 53-55 and 59 are rejected under 35 U.S.C. §101 as failing to accomplish a practical result and/or as being directed to non-statutory subject matter. This rejection is respectfully traversed.

As regards claims 1-33, 54 and 55, the Examiner asserts that independent claims 1 and 25 fail to recite a practical application because they "only' require a calculating step.. This assertion is incorrect. Claim 1 does not merely recite a calculating step. Instead claim 1 recites four steps. In particular, claim 1 recites thermally coupling a first heating device to a first sensing device, generating heat at the first heating device, measuring a change in at least one electrical characteristic of the first sensing device caused by the heat generated at the first heating device, and

calculating a temperature of the first heating device using the measured change in the at least one electrical characteristic. Only a clear disregard of the claim features could support the Examiner's conclusion that claim 1 only recites a calculating step and produces no tangible result.

MPEP 2106 (C)(2)(1) entitled "Practical Application by Physical Transformation" (page 2100-11) specifically states "USPTO personnel first shall review the claim and determine if it provides a transformation or reduction of an article to a different state or thing. If personnel find such a transformation or reduction, USPTO personnel shall end the inquiry and find that the claim meets the statutory requirement of 35 U.S.C. 101" (emphasis added), and without considering whether the invention produces a useful. Concrete or tangible result. As the Examiner must concede, at least the step of "thermally coupling a first heating device to a first sensing device" clearly transforms one thing into another thing or state because it physically connects (via thermal coupling) two tangible things, i.e., the first heating device and the first sensing device. Thus, the Examiner must end the inquiry and find that claim 1 meets the statutory requirement of 35 U.S.C. 101.

Claim 25 also does not merely recite a calculating step. Instead claim 25 recites five steps. In particular, claim 25 recites thermally coupling a heating transistor to a measurement transistor at one or more predetermined distance, calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature, generating heat at the heating transistor, incrementally measuring a change in the at least one electrical characteristic of the measurement transistor caused

by the heat generated at the heating transistor, and calculating a temperature of the heating transistor using the measured change in the at least one electrical characteristic. Again, only a clear disregard of the claim features could support the Examiner's conclusion that claim 25 only recites a calculating step. Furthermore, the Examiner must concede that at least the step of "thermally coupling a heating transistor to a measurement transistor at one or more predetermined distance" clearly transforms one thing into another thing or state because it physically connects (via thermal coupling) two tangible things, i.e., the heating transistor and a measurement transistor. Thus, the Examiner must end the inquiry and find that claim 1 meets the statutory requirement of 35 U.S.C. 101.

As regards claims 53 and 59, the Examiner asserts that independent claim 53 is directed to non-statutory subject matter apparently because it is directed to a computer program which is not a physical thing. This assertion is incorrect. Claim 53 also clearly recites a transformative step. For example, claim 53 specifically recites arranging a common source contact on a SiGe island, the common source contact leading to a source of both a first heating device and a first sensing device. A common source contact is clearly tangible, as is an SiGe island. Furthermore claim 53 recites measuring a change in at least one electrical characteristic of the first sensing device caused by heat generated at the first heating device. Clearly, the measuring of heat with the first sensing device is tangible and not merely an abstract concept. Accordingly, the Examiner's assertions are incorrect and unsupported by any proper basis in the MPEP or US patent law.

Accordingly, Applicants respectfully request that the above-noted rejection under 35 U.S.C. § 101 be withdrawn.

35 U.S.C. §102(e) Rejection

Claims 1-18, 24-35, 37-43 and 47-59 are rejected under 35 U.S.C. §102(e) as being anticipated by US Patent Application Publication No. 2004/0075140 to BALTES et al. This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because BALTES fails to teach each and every element of the claims.

In particular, independent claim 1 recites, *inter alia,*

> calculating a temperature of the first heating device using the measured change in the at least one electrical characteristic.

Additionally, independent claim 25 recites, *inter alia,*

> calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature;
> incrementally measuring a change in the at least one electrical characteristic of the measurement transistor caused by the heat generated at the heating transistor; and
> calculating a temperature of the heating transistor using the measured change in the at least one electrical characteristic.

Furthermore, independent claim 34 recites, *inter alia,*

> the transistor configured to generate heat and the transistor configured to sense temperature being arranged on the silicon island; and

a common source contact being arranged on the silicon island and leading to the source of both the transistor configured to generate heat and the transistor configured to sense temperature.

Still further, independent claim 39 recites, *inter alia,*

at least one sensing field effect transistor arranged within the at least one silicon island corresponding to each heating field effect transistor of the at least one heating field effect transistor, wherein each sensing field effect transistor is arranged a prescribed distance from its corresponding heating field effect transistor and each sensing field effect transistor is configurable to sense a temperature.

Moreover, independent claim 47 recites, *inter alia,*

three silicon sections;
three pairs of active regions, wherein each pair of active regions is arranged on a respective silicon section, wherein each pair of active regions is configurable to produce and sense heat; and
three thermal conductors, wherein each thermal conductor is arranged between each active region of each respective pair of active regions.

Finally, independent claim 53 recites, *inter alia,*

arrange a common source contact on a SiGe island, the common source contact leading to a source of both a first heating device and a first sensing device.

Applicants submit that BALTES does not disclose, or even suggest, at least these features.

Applicants acknowledge, for example, that BALTES discloses a device utilizing an Si island 12, a membrane 11, a poly-silicon resistor heater 13 arranged in the membrane 11, a plurality of temperature sensors 14 and 15 arranged at predetermined distances, and a plurality of contact electrodes 16 (see Fig. 3 and paragraphs [0074] – [[0079]). However, the Examiner has not identified any language in BALTES which discloses or suggests calculating a temperature of the first heating device using the measured change in the at least one electrical characteristic (claim 1). Applicants submit that BALTES instead (see paragraph [0083]) discloses that the various sensors

14.15 can measure "temperature distribution over the membrane" (emphasis added).

The Examiner identifies paragraph [0106] of BALTES as disclosing calculating a temperature of the first heating device using the measured change in the at least one electrical characteristic (claim 1). This is incorrect. Paragraph [0106] merely discloses the following:

> [0106] The temperature on the bulk chip is measured using the voltage difference of two Vbe junctions working at different current densities (Temp. 2). The expected accuracy of the measured temperature is about ± 1% after calibration. The resistance of the SnO_2 resistor (Sensor) is measured using a linear-to-logarithmic converter (Lin/Log) based on the exponential behavior of the Vbe junction.

While it is true that such language discusses measuring a temperature using a voltage difference, BALTES uses a poly-Si resistor temperature sensor (see paragraph [0105] to measure "[t]the temperature of the bulk chip", and does not calculate a temperature of the first heating device using the measured change in the at least one electrical characteristic (claim 1).

The Examiner has also failed to identify any language in BALTES which discloses or suggests calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature, much less, incrementally measuring a change in the at least one electrical characteristic of the measurement transistor caused by the heat generated at the heating transistor, and calculating a temperature of the heating transistor using the measured change in the at least one electrical characteristic (claim 25). Again, BALTES is apparently concerned with using the various sensors 14/15 to measure "temperature distribution over the membrane" (emphasis added) and not calculating a temperature of the heating transistor using the

measured change.

The Examiner identifies paragraphs [0077] and [0104] - [0106] of BALTES as disclosing calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature (claim 25). This is incorrect. Paragraphs [0077] and [0104] - [0106] merely discloses the following:

> [0077] The temperature of the chip 1 (FIG. 1) is expected to increase by approximately 4-6° C over ambient temperature due to the heat flow from the membrane 11. The thermal isolation seems to work well, since the dielectric membrane materials are good thermal insulators and the rather thick silicon chip acts as a heat sink. Consequently, heat transfer from the membrane 11 to the chip 1 is no problem.
>
> [0104] In the block diagram shown in FIG. 12, the temperature control of the membrane is implemented using an analog proportional controller. A digital PID (Proportional-Integrative-Derivative) controller may be used as alternative if more flexibility to the desired temperature waveform is desired. Using an embedded digital PID controller would even further improve the stability of the system and reduce the steady-state deviation. The routine operating temperature range of the membrane is from 200° C to 400° C.
>
> [0105] The temperature on the membrane is measured using a poly-Si resistor as temperature sensor (Temp. 1). The accuracy of the measured temperature is determined from experimental data, i.e. the known change of poly-Si resistivity at high temperatures. Additionally or alternatively, Pt-thermoresistors, which can be deposited on the membrane, may be used.
>
> [0106] The temperature on the bulk chip is measured using the voltage difference of two Vbe junctions working at different current densities (Temp. 2). The expected accuracy of the measured temperature is about .+-.1% after calibration. The resistance of the SnO_2 resistor (Sensor) is measured using a linear-to-logarithmic converter (Lin/Log) based on the exponential behavior of the Vbe junction.

While it is true that such language discusses measuring a temperature of a membrane and using a voltage difference, the noted language of BALTES merely discloses using a poly-Si resistor temperature sensor (see paragraph [0105]) to

measure "[t]the temperature of the bulk chip", and does not even remotely discuss calibrating the measurement transistor by measuring a particular electrical characteristic of an active region of the measurement transistor with the measurement transistor held at a known temperature, much less, incrementally measuring a change in the at least one electrical characteristic of the measurement transistor caused by the heat generated at the heating transistor (claim 25).

The Examiner has also neglected to identify any language in BALTES which discloses or suggests a transistor configured to generate heat and a transistor configured to sense temperature being arranged on the silicon island, much less, a common source contact being arranged on the silicon island and leading to the source of both the transistor configured to generate heat and the transistor configured to sense temperature (claim 34). The device shown in Fig. 3 of BALTES instead merely discloses a poly-silicon resistor heater 13 and various contacts 16 arranged on the membrane 11.

The Examiner identifies paragraphs [0036], [0038], [0072] and [0084] of BALTES as disclosing a transistor configured to generate heat and a transistor configured to sense temperature being arranged on the silicon island and a common source contact being arranged on the silicon island and leading to the source of both the transistor configured to generate heat and the transistor configured to sense temperature (claim 34). This is incorrect. Paragraph [0036] merely discusses how a FET can be used as a heater to dynamically control the temperature of a membrane. Paragraph [0038] merely discusses how the disclosed chip can include a sensor with heating elements. Paragraph [0072] merely discusses the cross-section of the membrane. Finally,

paragraph [0084] merely discusses how temperature sensors can be integrated to monitor a heat distribution. Such disclosure, however, is silent with regard to a transistor configured to generate heat and a transistor configured to sense temperature being arranged on the silicon island, much less, a common source contact being arranged on the silicon island and leading to the source of both the transistor configured to generate heat and the transistor configured to sense temperature (claim 34).

The Examiner has also neglected to identify any language in BALTES which discloses or suggests at least one sensing field effect transistor arranged within the at least one silicon island corresponding to each heating field effect transistor of the at least one heating field effect transistor, wherein each sensing field effect transistor is arranged a prescribed distance from its corresponding heating field effect transistor and each sensing field effect transistor is configurable to sense a temperature (claim 39). Again, the device shown in Fig. 3 of BALTES instead merely discloses a poly-silicon resistor heater 13 and that the sensor 14 is arranged within the membrane 11 and not the Si island 12.

The Examiner also identifies paragraphs [0036], [0038], [0072] and [0084] of BALTES as disclosing at least one sensing field effect transistor arranged within the at least one silicon island corresponding to each heating field effect transistor of the at least one heating field effect transistor, wherein each sensing field effect transistor is arranged a prescribed distance from its corresponding heating field effect transistor and each sensing field effect transistor is configurable to sense a temperature (claim 39). This is incorrect. Again, paragraph [0036] merely discusses how a FET can be used as a heater to dynamically control the temperature of a membrane. Paragraph

[0038] merely discusses how the disclosed chip can include a sensor with heating elements. Paragraph [0072] merely discusses the cross-section of the membrane. Finally, paragraph [0084] merely discusses how temperature sensors can be integrated to monitor a heat distribution. Such disclosure, however, is silent with regard to at least one sensing field effect transistor arranged within the at least one silicon island corresponding to each heating field effect transistor of the at least one heating field effect transistor, wherein each sensing field effect transistor is arranged a prescribed distance from its corresponding heating field effect transistor and each sensing field effect transistor is configurable to sense a temperature (claim 39).

The Examiner has also failed to demonstrate that BALTES discloses or suggests three silicon sections, three pairs of active regions, wherein each pair of active regions is arranged on a respective silicon section, wherein each pair of active regions is configurable to produce and sense heat, and three thermal conductors, wherein each thermal conductor is arranged between each active region of each respective pair of active regions (claim 47). Instead, the device shown in Fig. 3 of BALTES discloses one active region having a poly-silicon resistor heater 13, sensors 14/15, contacts 16, a membrane 11, and an Si island 12.

The Examiner also identifies paragraph [0075] of BALTES as disclosing three silicon sections, three pairs of active regions, wherein each pair of active regions is arranged on a respective silicon section, wherein each pair of active regions is configurable to produce and sense heat, and three thermal conductors, wherein each thermal conductor is arranged between each active region of each respective pair of active regions (claim 47). This is incorrect. Paragraph [0075] merely states the

following:

> [0075] Also, different temperature sensors may be used. Shown in FIG. 3 are a central temperature sensor 14 and an off-membrane temperature sensor 15. To achieve the desired resistive temperature measurement, Al, poly-Si and/or n-Si diffusion resistors may be placed on the membrane. A plurality of sensors may be distributed over the heated area for measuring lateral temperature variations. A thermopile configuration may also be used. Also, the bulk chip temperature of the chip shown in FIG. 1 (not the membrane) can be measured either resistively or by an integrated active temperature sensor circuit.

While it is true that such language discusses using various temperature distributed sensors to measure a temperature of a membrane, the noted language of BALTES merely discloses using a poly-Si resistor temperature sensor to measure "[t]the temperature of the bulk chip" (see paragraph [0106]), and does not even remotely discuss three silicon sections, three pairs of active regions, wherein each pair of active regions is arranged on a respective silicon section, wherein each pair of active regions is configurable to produce and sense heat, and three thermal conductors, wherein each thermal conductor is arranged between each active region of each respective pair of active regions (claim 47).

Finally, the Examiner has failed to demonstrate that BALTES discloses or suggests a common source contact arranged on a SiGe island, wherein the common source contact leads to a source of both a first heating device and a first sensing device (claim 53). The device shown in Fig. 3 of BALTES instead merely discloses a poly-silicon resistor heater 13, temperature sensors 14/15, and various contacts 16 arranged in the membrane 11 and not on the Si island 12, much less, an SiGe island.

Applicants note, in particular, that independent claim 53, and dependent claims 54-58 are not even mentioned on pages 4-6 of the instant Office Action.

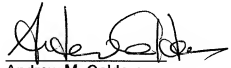
Thus, Applicants respectfully submit that independent claims 1, 25, 34, 39, 47 and 53, and dependent claims 2-18, 24, 26-33, 35, 37, 38, 40-43, 48-52 and 54-59 are allowable.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(e) should be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0456** (Burlington).

Respectfully submitted,
Paul A. HYDE et al.



Andrew M. Calderon
Reg. No. 38,093

February 26, 2007
Greenblum & Bernstein, P.L.C.
September 4, 2006
1950 Roland Clarke Place
Reston, Virginia 20191
Telephone: 703-716-1191
Facsimile: 703-716-1180